Developing machines with nanometer accuracy

How COMSOL is used as one of the enablers

Fred Huizinga
Group Leader Mechanical Analysis
October 2016
History of ASML
Founded in 1984 as a spin-off from Philips
History of ASML
Nowadays: A Global Presence

3,400 employees
8,800 employees
2,800 employees

Over 70 sales and service offices located worldwide

Source: ASML Q2 2016
What do we do?
A market of 12 large ASML customers

<table>
<thead>
<tr>
<th>Company</th>
<th>2015 semi capex (est., $M)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Samsung</td>
<td>13,000</td>
</tr>
<tr>
<td>TSMC Group</td>
<td>9,000</td>
</tr>
<tr>
<td>Intel</td>
<td>7,200</td>
</tr>
<tr>
<td>SK Hynix</td>
<td>4,700</td>
</tr>
<tr>
<td>Globalfoundries</td>
<td>4,000</td>
</tr>
<tr>
<td>Micron Technology</td>
<td>3,800</td>
</tr>
<tr>
<td>Toshiba (incl. SanDisk)</td>
<td>3,095</td>
</tr>
<tr>
<td>Sony</td>
<td>1,991</td>
</tr>
<tr>
<td>Inotera Memories</td>
<td>1,836</td>
</tr>
<tr>
<td>United Microelectronics Group</td>
<td>1,800</td>
</tr>
<tr>
<td>SMIC Group</td>
<td>1,500</td>
</tr>
<tr>
<td>Infineon Technologies</td>
<td>896</td>
</tr>
</tbody>
</table>

Guidance for next quarter (Q3)
- Q3 net sales approximately €1.7 billion
- Gross margin around 47%

Full year 2016 sales
- Expected to exceed our 2015 record sales
The Microchip Manufacturing Process
All process steps

Repeat 30 to 40 times to build 3 dimensional structure
The Microchip Manufacturing Process
The machine in action

- Reticle Stage
- Wafer Stage
The Microchip Manufacturing Process
The machine in action
The challenge
Keeping up with “Moore’s Law”

Who is Gordon Moore?:
- Born 3 January 1929, San Francisco, California, USA
- Got a BSc (1950) and PhD (1954) in chemistry
- Is one of the founders of both Fairchild Semiconductors (1957) and Intel (1968)
- His is now 87 years old and lives in Hawaii

What did Moore state in 1965?
- The complexity for minimum component costs will increased at a rate of roughly a factor of two per year

G. Moore, "Cramming more components onto integrated circuits" Electronics, Vol. 38, No. 8 (1965)

Interview with ASML: https://www.youtube.com/watch?v=EzyJxAP6AQo
The challenge
Keeping up with “Moore’s Law”

Retrospective...
Mobile devices and Gaming Consoles are most demanding

Source: Samsung ISSCC 2015
The challenge
Keeping up with “Moore’s Law”
Computations per Kilowatt hour double every 1.5 years

Source: Jonathan Koomey, Lawrence Berkeley National Laboratory and Stanford University, 2009

Regression results:
N = 76
Adjusted R-squared = 0.983
Comps/kWh = exp(0.440243 x year – 849.259)
Average doubling time (1946 to 2009) = 1.57 years

Moore’s Paper

Computations per kWh
The challenge
Keeping up with “Moore’s Law”

- Memory: ×8000
- Weight: ÷40000
- Price: ÷50000
- Processing power: ×6 – 230
- Electrical Power: ÷30000

Cray 1, the first supercomputer:
- 8 MB memory
- 5.5 tons
- 150 kW (Freon cooled)
- $8.66 Million ($25 Million today)
- 3.4 – 134 Mflops

Today’s phone:
- 64 GB memory
- 130 g (incl. 13 megapixel camera with full HD video)
- 1-6 W
- $500,00
- 791 Mflops
The challenge
How to keep up with Moore’s law

The iPhone A8 Processor
CD= Critical Dimension

A 300 mm Wafer
The challenge
How to keep up with Moore’s law

Designing for nanometer accuracy; to create some awareness...

Have a 300 mm wafer magnified to approximately the size of The Netherlands, then...
- CD would be about 15 mm
- And overlay accuracy 4 mm
The challenge
How to keep up with Moore’s law
Designing for nanometer accuracy; to create some awareness...

• A **human hair** measures about 80 micrometer, 5300 times bigger than CD

• A **flue virus** measures about 100 nm, almost 6
time bigger than CD

• Overlay performance for EUV is
  1 nanometer, less than **5 Si atoms**!

→ Dust is “killing” for the lithography process!

Source: Building quantum states with individual silicon atoms, Sciencedaily.com,
The challenge
How to keep up with Moore’s law

How to print smaller lines → shorter wavelength of the light

\[ CD = k_1 \cdot \frac{\lambda}{NA} \]

<table>
<thead>
<tr>
<th>Wavelength</th>
<th>Year</th>
<th>Platform</th>
</tr>
</thead>
<tbody>
<tr>
<td>13.5 nm</td>
<td>2011</td>
<td>EUV</td>
</tr>
<tr>
<td>193 nm</td>
<td>2003</td>
<td>Immersion</td>
</tr>
<tr>
<td>248 nm</td>
<td>1992</td>
<td>PAS 5500</td>
</tr>
<tr>
<td>365 nm</td>
<td>1986</td>
<td>PAS 5000</td>
</tr>
<tr>
<td>436 nm</td>
<td>1984</td>
<td>PAS 2000</td>
</tr>
</tbody>
</table>
How to keep up with Moore’s law
The future of lithography: EUV

Wavelength: 13.5 nanometers
Resolution: ≤ 22 nanometers
Overlay: 1.0 nanometers
Wafer size: 300 mm
Productivity: 125 wafers per hour

13.5 nm, close to X-rays (starts at 10nm). Major implications for the design of the machine.
How to keep up with Moore’s law
The future of lithography: EUV

EUV light is absorbed by air and lenses!
How to keep up with Moore’s law
The future of lithography: EUV

We need to maintain a clean vacuum, but every time we expose a wafer, the photoresist releases trillions of particles.

EUV mirrors are polished to an accuracy of ~50 picometers – less than the diameter of a silicon atom.

Blown up to the size of the Netherlands, the biggest difference in height would be less than a millimeter.
How to keep up with Moore’s law
The future of lithography: EUV

Laser-Produced Plasma (LPP) source

- Each tin droplet is precisely hit by a drive laser pulse to bring it in a plasma phase
- 40,000 times per second...
### Use of CAE within Development & Engineering

#### Physics / areas of application

<table>
<thead>
<tr>
<th>Electrical</th>
<th>Mechanical</th>
<th>Fluid</th>
<th>Chemical</th>
<th>Other</th>
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</thead>
<tbody>
<tr>
<td>AC/DC</td>
<td>Structural Mechanics</td>
<td>CFD</td>
<td>Molecular Dynamics</td>
<td>Motion &amp; Thermal Control</td>
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<tr>
<td>Wave Optics</td>
<td>Structural Dynamics</td>
<td>Molecular Flow</td>
<td>....</td>
<td>Optimization</td>
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<td>Ray Optics</td>
<td>Heat Transfer</td>
<td>Microfluidics</td>
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<td>....</td>
<td>Multibody Dynamics</td>
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<td>Fatigue</td>
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<tr>
<td>....</td>
<td>Acoustics</td>
<td>....</td>
<td>....</td>
<td>....</td>
</tr>
</tbody>
</table>

*Not pretending to be complete*
Use of CAE within Development & Engineering

Software used

ELECTRICAL  MECHANICAL  FLUID  CHEMICAL  OTHER

HyperLith™  ANSYS®  ANSYS®  FLUENT®  MATLAB®

Mentor Graphics  COMSOL  GROMACS®  OpenFOAM

Photon Engineering  Opera  Altair HyperWorks®  CD-adapco

VirtualLab™  SIEMENS  eSI

Zemax  Sigmadyne™ SigFit

Not pretending to be complete
Use of CAE within Development & Engineering
Trends and developments

• More complex systems, while ever tighter requirements have to be met. At the same time Time to Market should be shorter while quality should not be compromised → Time to Maturity mindset
• Requirements on System/Module level are a fraction of the requirements on Machine level → analysis on sub-nanometer level (moving into analysis on pico-meter scale)
• Evolution from “single physics” to “multi physics”
• Verification by physical testing becomes more difficult, not feasible or even not possible.
• Higher demand on CAE: Bigger models, more advanced models, more simulations
Use of CAE within Development & Engineering  
How do we anticipate

PEOPLE development

• Develop Engineers that are “CAE competent” and let them analyze their own designs (up to a certain level) → Co-operation with NAFEMS on training and PSE Certification*
• Provide user friendly “Simulation App’s” to Design Engineers

*NAFEMS Juli 2016 Benchmark magazine
Use of CAE within Development & Engineering
How do we anticipate

**PROCESS**

- Tighter Integration of Virtual Verification into the development process
- Define/optimize the CAE “WoW”
  ("Way-of-Working", not Warcraft)

- SPDM (Simulation Process and Data Management)
Use of CAE within Development & Engineering

How do we anticipate

TOOLS & METHODS

• Increase “Analysis Maturity” to enable more verification by analysis
• HPC Cluster. Currently several thousands of cores and a number of GPU enhanced nodes in addition. Used globally.
• Optimization and stochastic analysis
• Multi-physics analysis → COMSOL Multiphysics
Use of COMSOL within Development & Engineering

Example: Air Bearing Analysis

- Air Bearings are used in our machines at many places because of
  - High stiffness $\rightarrow$ high positional accuracy is attainable
  - No friction $\rightarrow$ no wear (no particles!)
  - High load bearing capacity in a small volume
  - Thermal isolation
  - ...

- Typical design criteria
  - Stiffness (translational and rotational)
  - Gap size under load (“fly height”)
  - Air consumption

\[ D_C = 0.268 \text{m} \]
\[ D_p = 0.228 \text{m} \]
\[ D_m = 0.139 \text{m} \]

Thin $\approx 10 \mu \text{m}$ Air film
Use of COMSOL within Development & Engineering

Example 2: Air Bearing Analysis

Air film only analysis (structure assumed to be very stiff) with **Air Bearing Calculator**

- Takes away the effort of FEM modelling, analysis set-up and post-processing

[Main page: Select configuration:]

1. Rectangular/Cylindrical flat Air Bearing
2. Cylindrical/Conical Air Bearing
3. Under development: Flat Porous Air Bearing
Use of COMSOL within Development & Engineering
Example: Air Bearing Analysis

Air film only analysis (structure assumed to be very stiff)
- Input dimensions and other variables and results page
- Will be made available to more engineers via COMSOL Application Server
Use of COMSOL within Development & Engineering
Under development: Wafer Load Simulation

- Multi Physics problem:
  - (Wafer) Dynamics
  - Flow
  - Contact mechanics
  - Thermal
  - Electrostatics
  - Motion Control
Questions?