



ASML

Developing machines with nanometer accuracy

How COMSOL is used as one of the enablers

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October 2016

Founded in 1984 as a spin-off from Philips



History of ASML

Nowadays: A Global Presence



Source: ASML Q2 2016

Over 70 sales and service offices located worldwide

What do we do?

A market of 12 large ASML customers



Guidance for next quarter (Q3)

- Q3 net sales approximately € 1.7 billion
- Gross margin around 47%

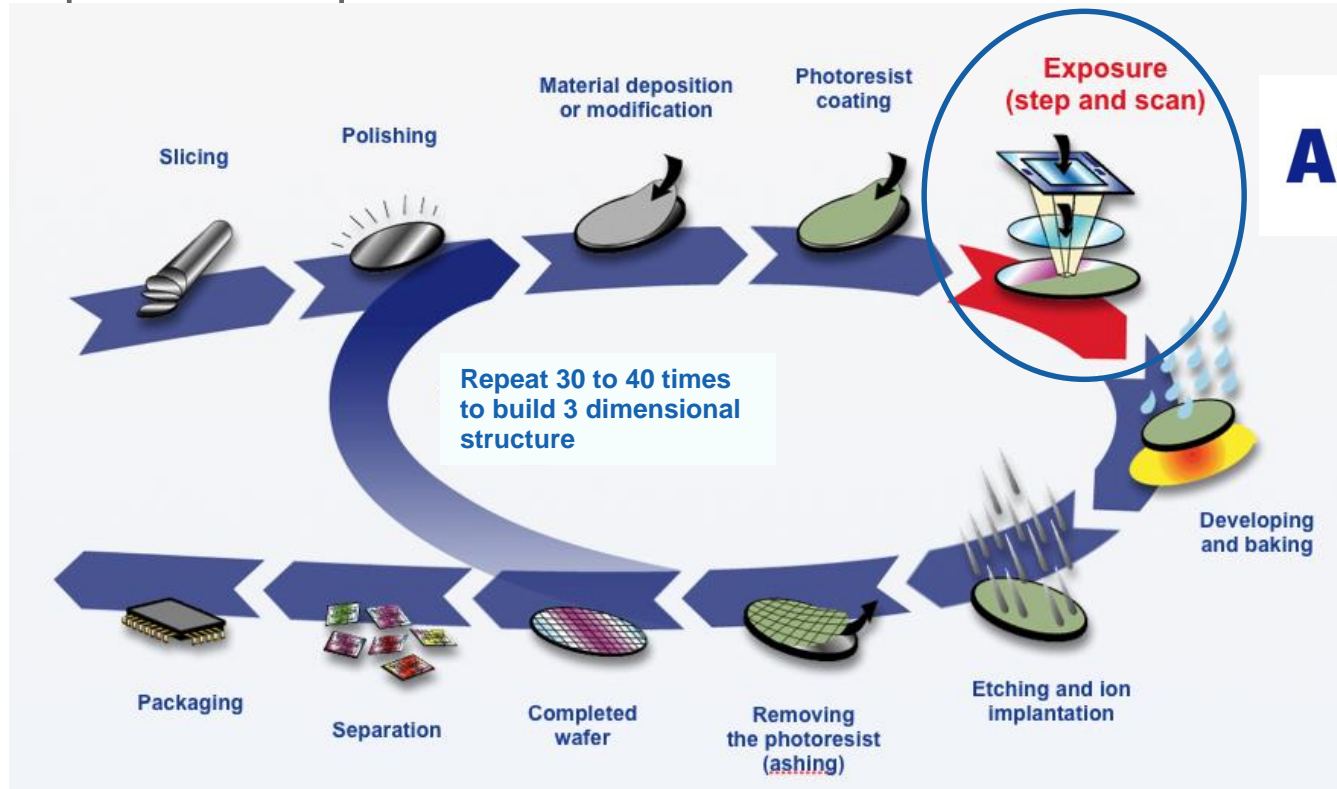
Full year 2016 sales

- Expected to exceed our 2015 record sales

Company	2015 semi capex (est., \$M)
Samsung	13,000
TSMC Group	9,000
Intel	7,200
SK Hynix	4,700
Globalfoundries	4,000
Micron Technology	3,800
Toshiba (incl. SanDisk)	3,095
Sony	1,991
Inotera Memories	1,836
United Microelectronics Group	1,800
SMIC Group	1,500
Infineon Technologies	896

The Microchip Manufacturing Process

All process steps



The Microchip Manufacturing Process

The machine in action

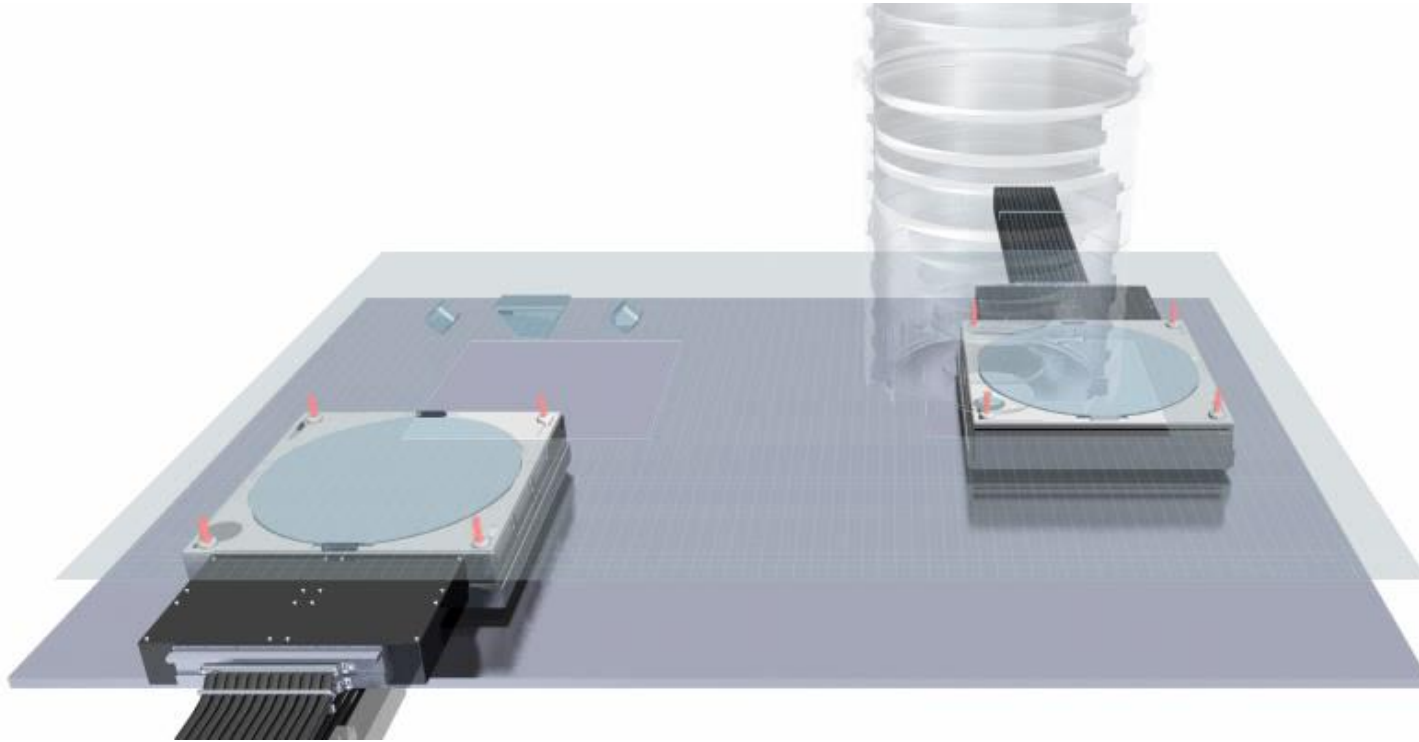


Reticle Stage

Wafer Stage

The Microchip Manufacturing Process

The machine in action



The challenge

Keeping up with “Moore’s Law”

Who is Gordon Moore?:

Andy

- Born 3 January 1929, San Francisco, California, USA
- Got a BSc (1950) and PhD (1954) in chemistry
- Is one of the founders of both Fairchild Semiconductors (1957) and Intel (1968)
- His is now 87 years old and lives in Hawaii

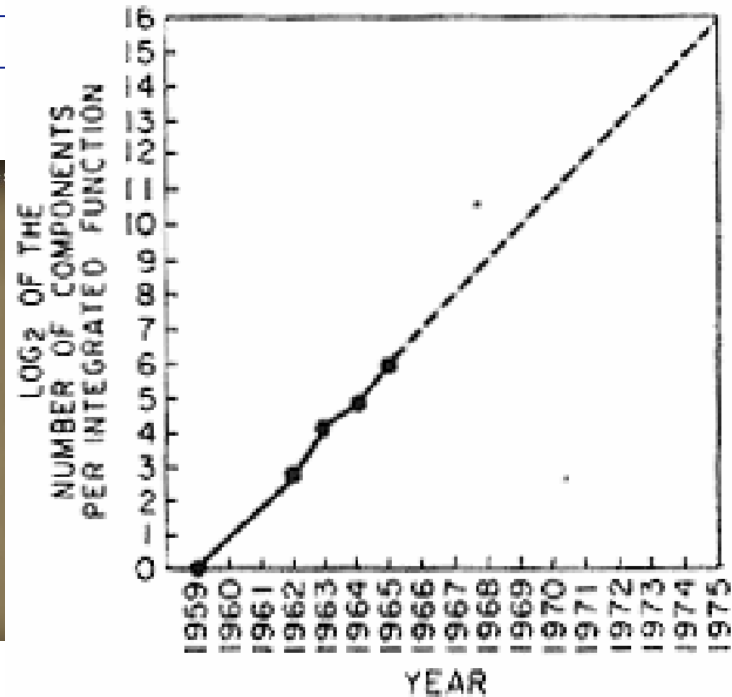
What did Moore state in 1965?

- The **complexity for minimum component costs** will increase at a rate of roughly a **factor of two per year**

Interview with

ASML: <https://www.youtube.com/watch?v=EzyJxAP6AQo>

G. Moore, “Cramming more components onto integrated circuits”
Electronics, Vol. 38, No. 8 (1965)



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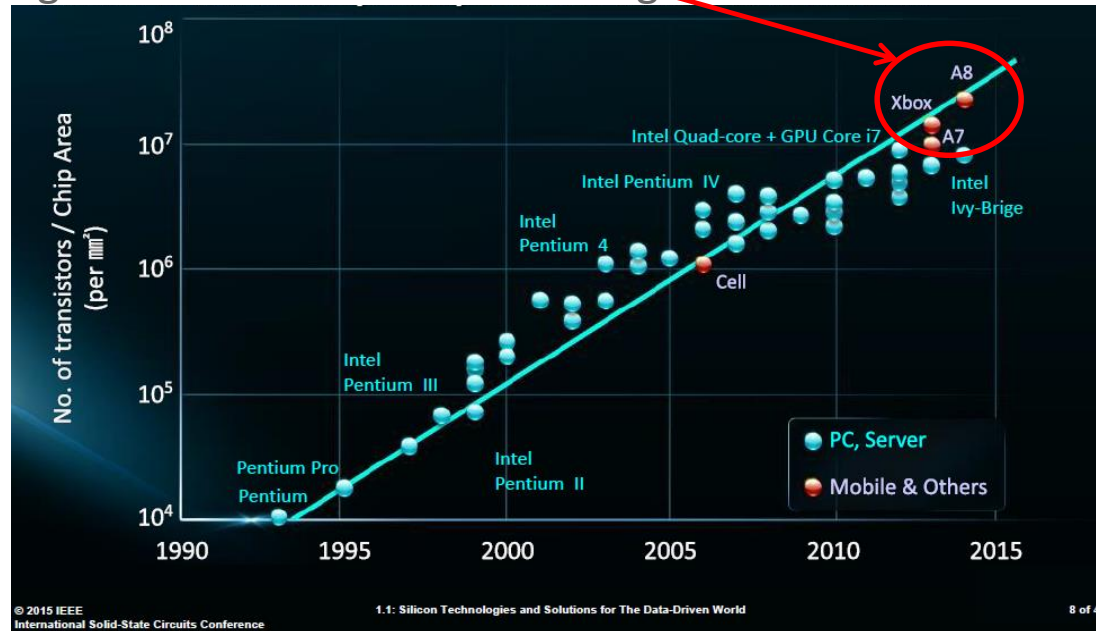
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The challenge

Keeping up with “Moore’s Law”

Retrospective...

Mobile devices and Gaming Consoles are most demanding



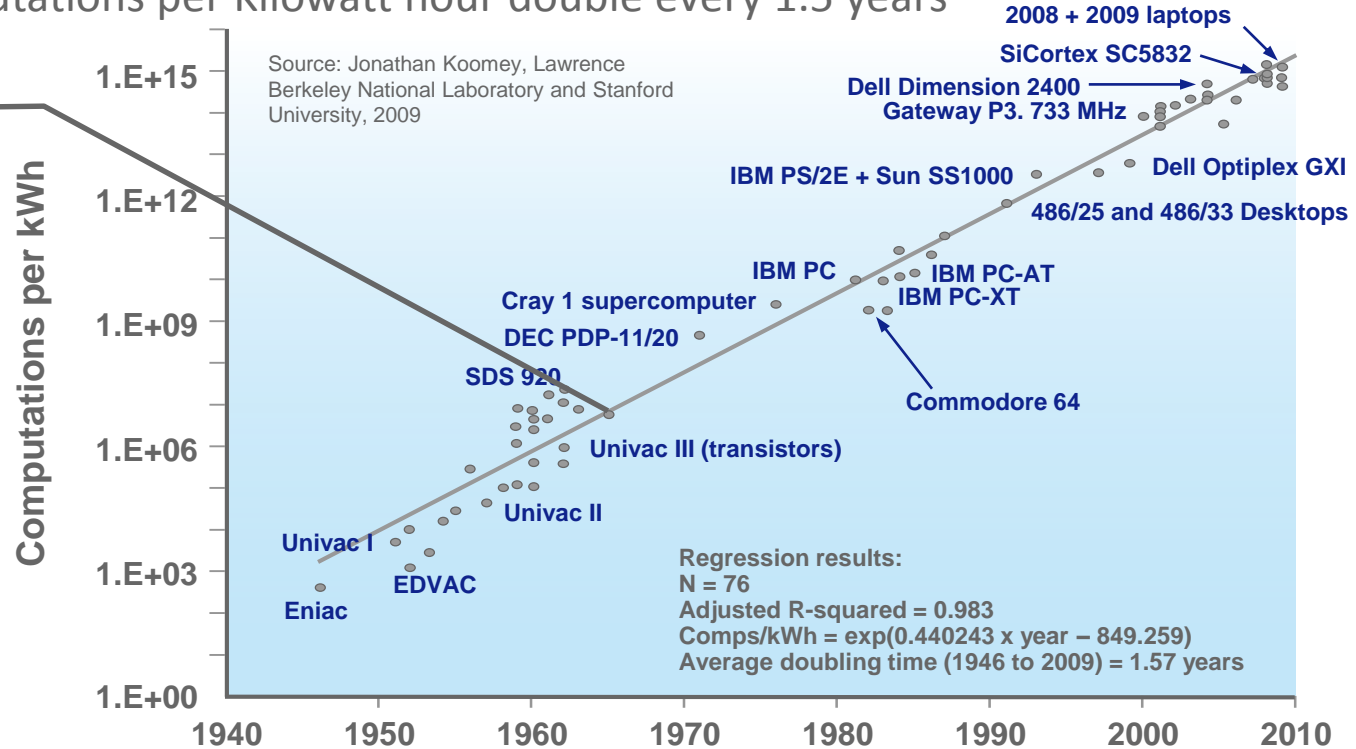
Source: Samsung ISSCC 2015

The challenge

Keeping up with “Moore’s Law”

Computations per Kilowatt hour double every 1.5 years

Moore’s Paper



The challenge

Keeping up with “Moore’s Law”

Memory: $\times 8000$
Weight: $\div 40000$
Price: $\div 50000$
Processing power: $\times 6 - 230$
Electrical Power: $\div 30000$



1976

Cray 1, the first supercomputer:

- 8 MB memory
- 5.5 tons
- 150 kW (Freon cooled)
- \$8.86 Million (\$25 Million today)
- 3.4 – 134 Mflops



2013

Today's phone:

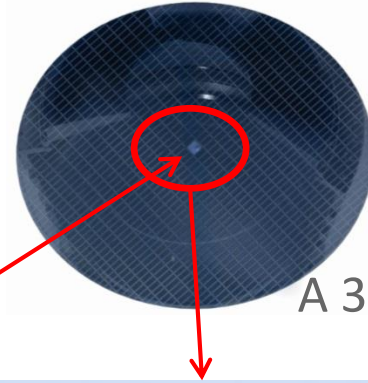
- 64 GB memory
- 130 g (incl. 13 megapixel camera with full HD video)
- 1-6 W
- \$ 500,00
- 791 Mflops

The challenge

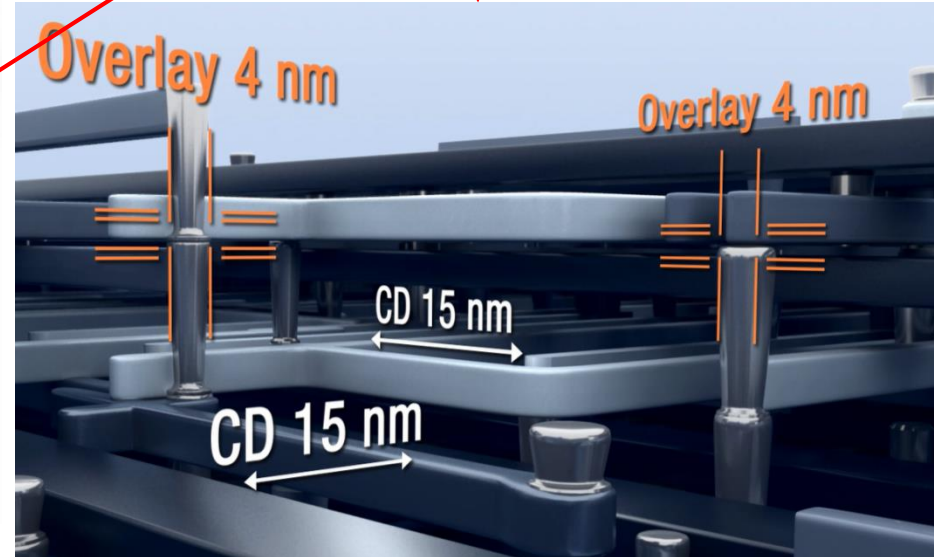
How to keep up with Moore's law

The iPhone A8 Processor

CD= Critical Dimension



A 300 mm Wafer



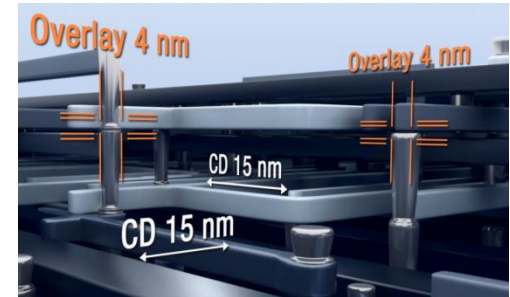
The challenge

How to keep up with Moore's law

Designing for nanometer accuracy; to create some awareness...


Have a 300 mm wafer magnified to approximately the size of The Netherlands, then...

- CD would be about 15 mm
- And overlay accuracy 4 mm



How to keep up with Moore's law

- A **human hair** measures about 80 micrometer, 5300 times bigger than CD
- A **flu virus** measures about 100 nm, almost 6 times bigger than CD
- Overlay performance for EUV is 1 nanometer, less than **5 Si atoms!**

A scanning electron micrograph (SEM) showing a textured surface, likely a virus or a material at the nanoscale. A white double-headed arrow is overlaid on the image, indicating a scale of 100 nm.

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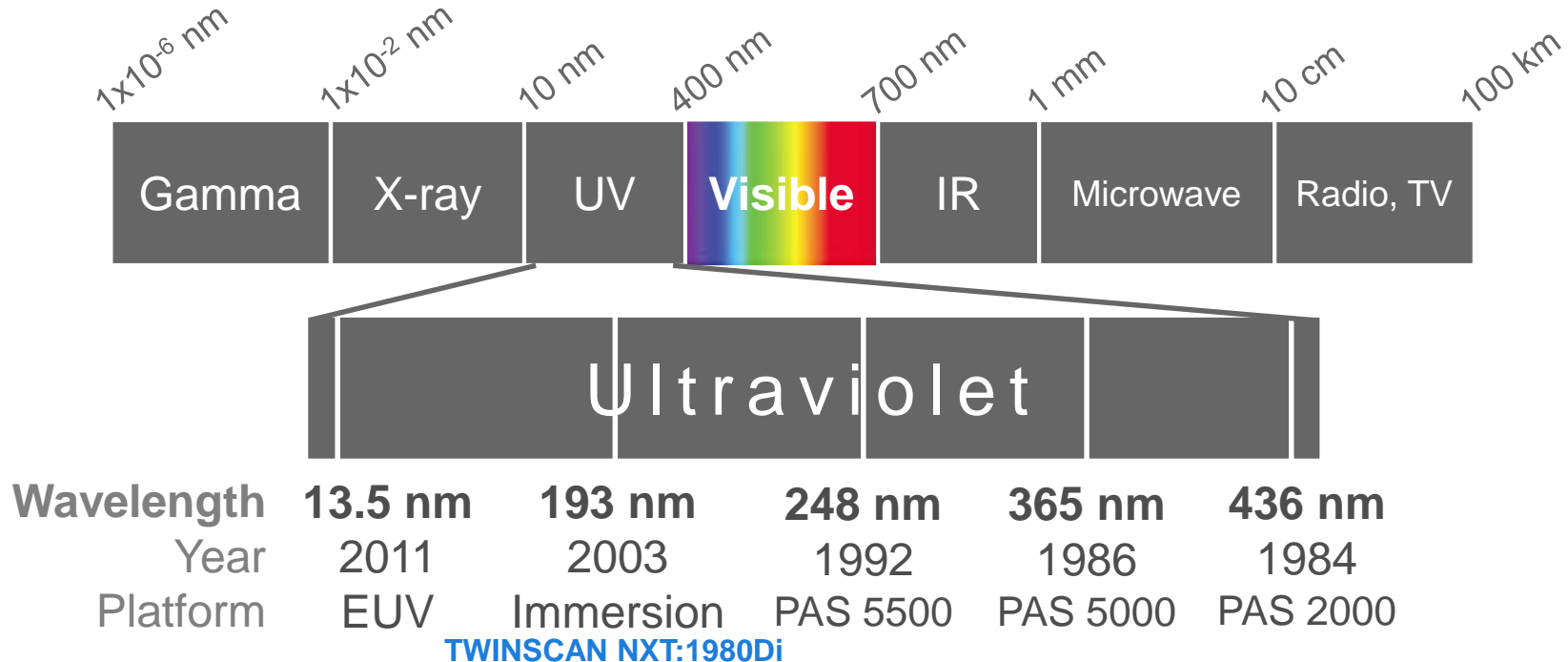


The challenge

How to keep up with Moore's law

$$CD = k_1 * \frac{\lambda}{NA}$$

How to print smaller lines → shorter wavelength of the light



How to keep up with Moore's law

The future of lithography: EUV

Wavelength:
13.5 nanometers

Resolution:
 ≤ 22 nanometers

Overlay:
1.0 nanometers

Wafer size:
300 mm

Productivity:
125 wafers per hour



13.5 nm, close to X-rays (starts at 10nm).
Major implications for the design of the machine

1984

PAS 2000

ASML's first stepper

2015

TWINSKAN NXT:1980Di

Our most advanced
immersion system

2015

TWINSKAN NXE:3350B

Production-ready EUV system

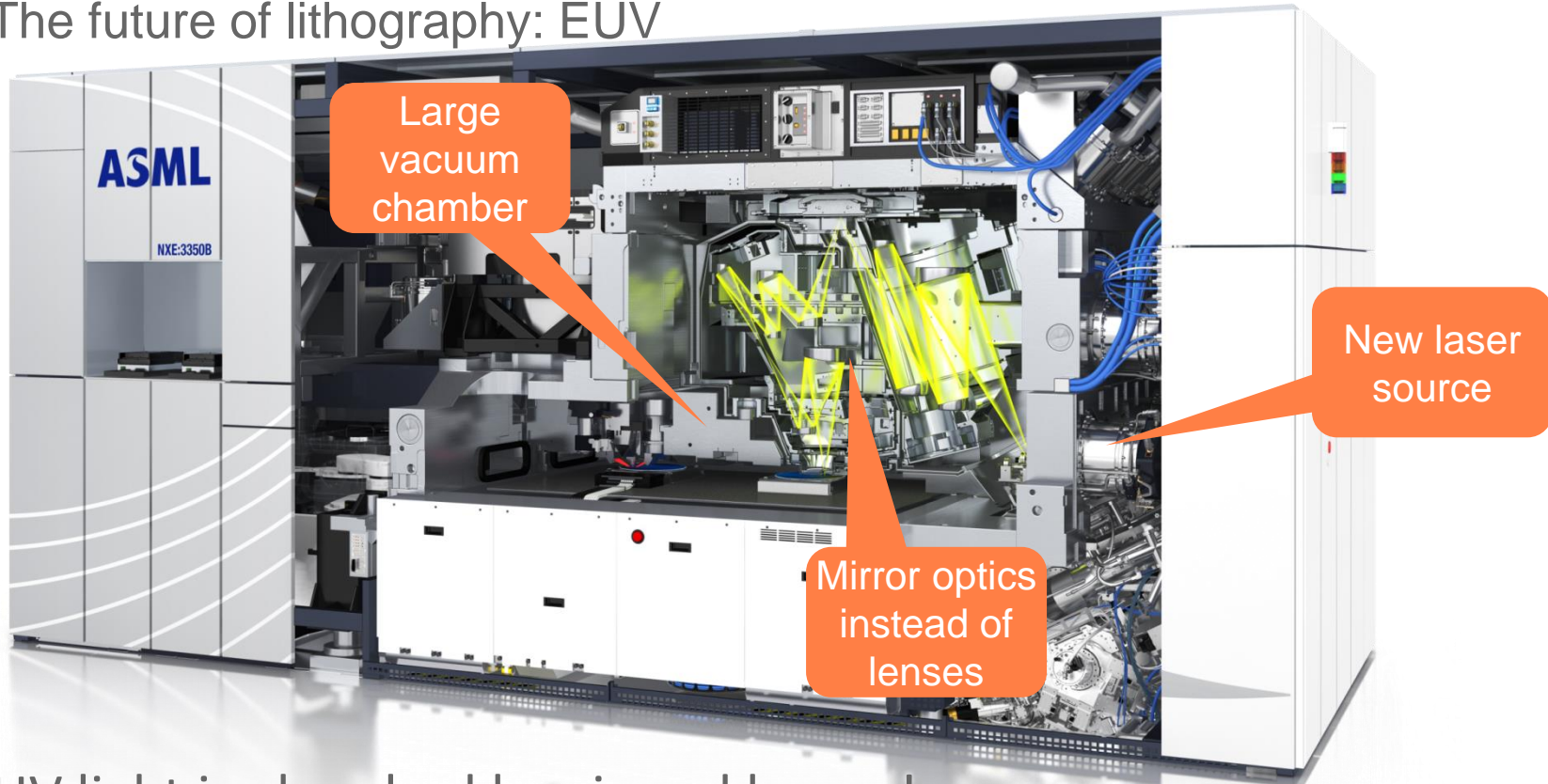
How to keep up with Moore's law

The future of lithography: EUV

Public

Slide 17

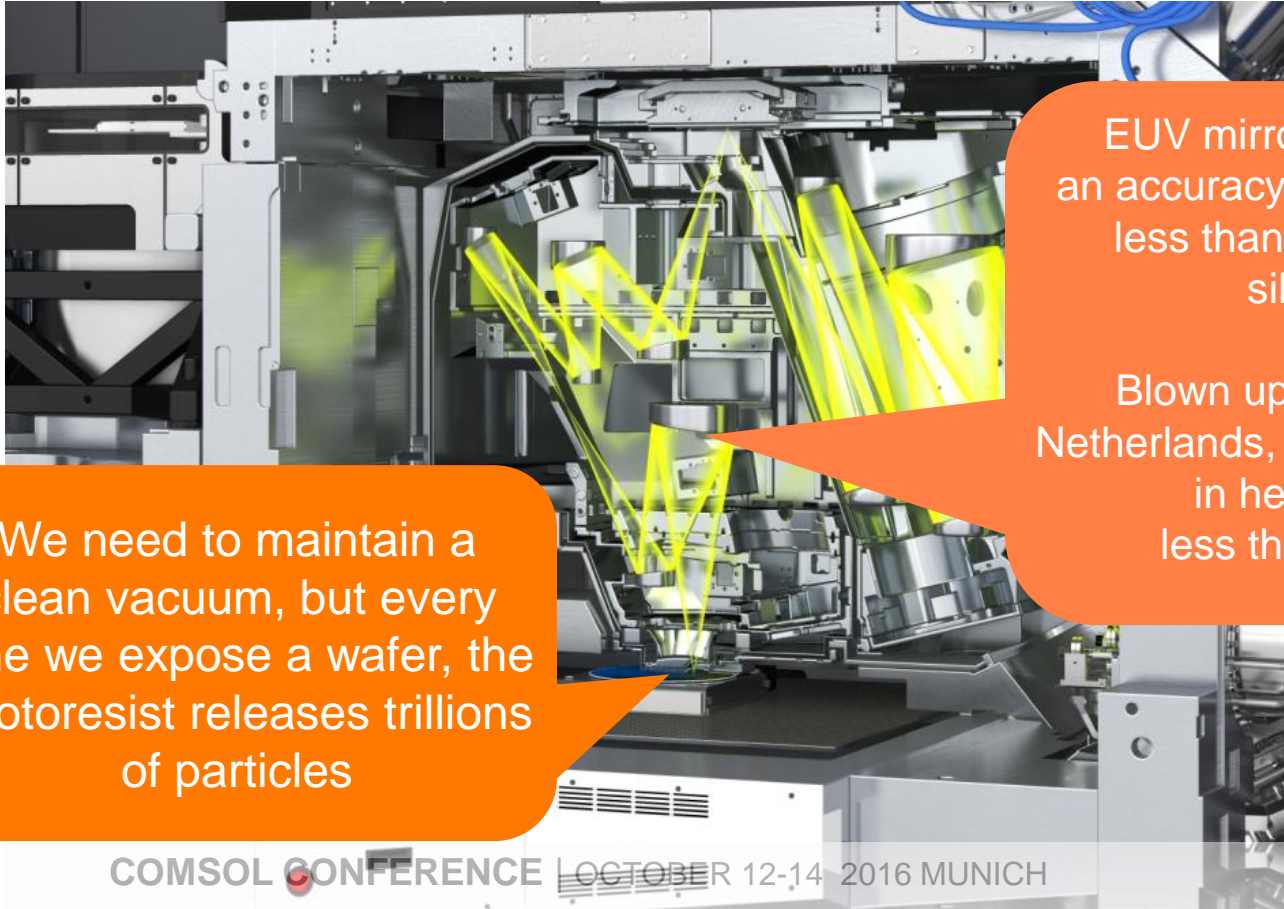
20 January 2016



EUV light is absorbed by air and lenses!

How to keep up with Moore's law

The future of lithography: EUV



We need to maintain a clean vacuum, but every time we expose a wafer, the photoresist releases trillions of particles

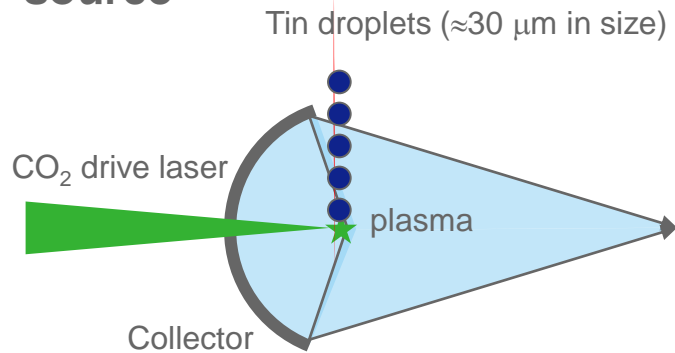
EUV mirrors are polished to an accuracy of ~ 50 picometers – less than the diameter of a silicon atom.

Blown up to the size of the Netherlands, the biggest difference in height would be less than a millimeter.

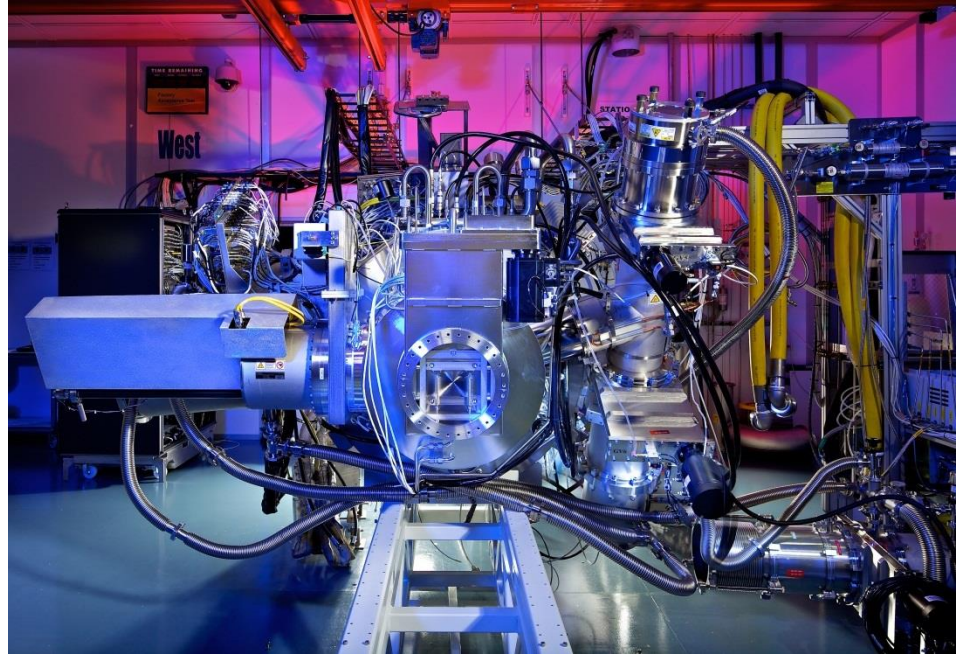
How to keep up with Moore's law

The future of lithography: EUV

Laser-Produced Plasma (LPP) source



- Each tin droplet is precisely hit by a drive laser pulse to bring it in a plasma phase
- 40,000 times per second...



Use of CAE within Development & Engineering

Physics / areas of application

ELECTRICAL	MECHANICAL	FLUID	CHEMICAL	OTHER
AC/DC	Structural Mechanics	CFD	Molecular Dynamics	Motion & Thermal Control
Wave Optics	Structural Dynamics	Molecular Flow	Optimization
Ray Optics	Heat Transfer	Microfluidics	
....	Multibody Dynamics		
	Fatigue		
	Acoustics			

Not pretending to
be complete

Use of CAE within Development & Engineering

Software used

ELECTRICAL

MECHANICAL

FLUID

CHEMICAL

OTHER

HyperLith™ANSYS®ANSYS®
FLUENT®MATLAB®
The Language of Technical ComputingMentor
Graphics®COMSOLGROMACS FAST.
FLEXIBLE.
FREE.Opera
Simulation Software
COBHAMPhoton
ENGINEERINGOpenFOAMAltair | HyperWorks®CD-adapcoMathcad®LightTrans
VirtualLab™SIEMENSesiZemaxSigmadyne™ SigFit

Not pretending to
be complete

Use of CAE within Development & Engineering

Trends and developments

- More complex systems, while ever tighter requirements have to be met. At the same time **Time to Market** should be shorter while quality should not be compromised → **Time to Maturity** mindset
- Requirements on System/Module level are a fraction of the requirements on Machine level → analysis on sub-nanometer level (moving into analysis on pico-meter scale)
- Evolution from “single physics” to “multi physics”
- Verification by physical testing becomes more difficult, not feasible or even not possible.
- Higher demand on CAE: Bigger models, more advanced models, more simulations

Use of CAE within Development & Engineering

How do we anticipate

PEOPLE development



- Develop Engineers that are “CAE competent” and let them analyze their own designs (up to a certain level) → Co-operation with NAFEMS on training and PSE Certification*
- Provide user friendly “Simulation App’s” to Design Engineers

*NAFEMS Juli 2016 Benchmark magazine

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ASML

Public

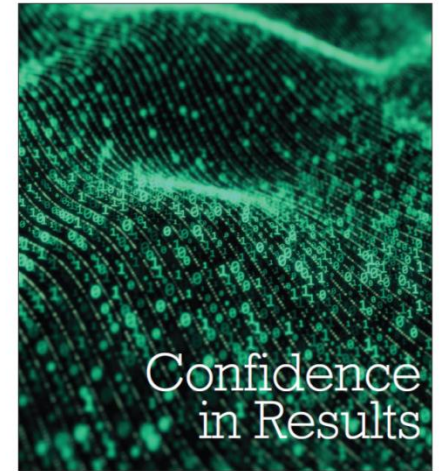
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20 October 2016



**BENCH
MARK**

THE INTERNATIONAL MAGAZINE FOR ENGINEERING DESIGNERS & ANALYSTS FROM NAFEMS



Use of CAE within Development & Engineering

How do we anticipate

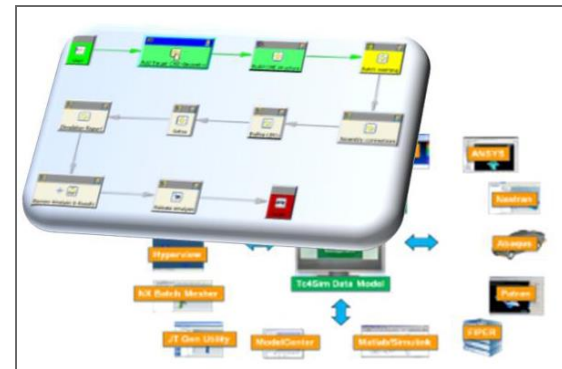
PROCESS



- Tighter Integration of Virtual Verification into the development process
- Define/optimize the CAE “WoW”

(“Way-of-Working”, not ~~WORLD OF Warcraft~~)

- SPDM (Simulation Process and Data Management)



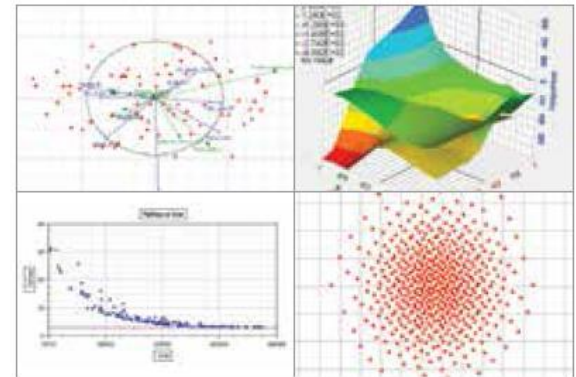
Use of CAE within Development & Engineering

How do we anticipate

TOOLS & METHODS



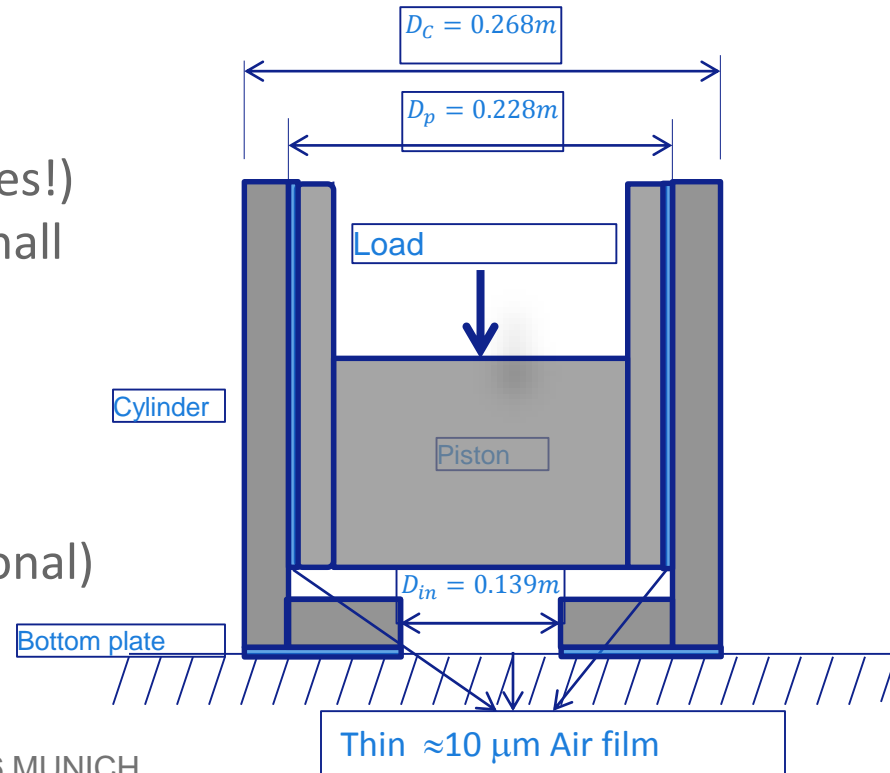
- Increase “Analysis Maturity” to enable more verification by analysis
- HPC Cluster. Currently several thousands of cores and a number of GPU enhanced nodes in addition. Used globally.
- Optimization and stochastic analysis
- Multi-physics analysis → **COMSOL Multiphysics**



Use of COMSOL within Development & Engineering

Example: Air Bearing Analysis

- Air Bearings are used in our machines at many places because of
 - High stiffness → high positional accuracy is attainable
 - No friction → no wear (no particles!)
 - High load bearing capacity in a small volume
 - Thermal isolation
 - ...
- Typical design criteria
 - Stiffness (translational and rotational)
 - Gap size under load (“fly height”)
 - Air consumption



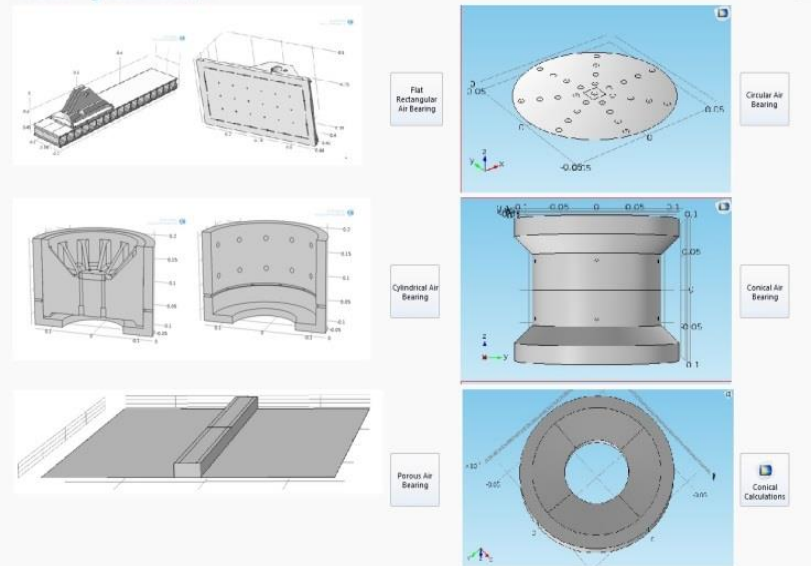
Use of COMSOL within Development & Engineering

Example 2: Air Bearing Analysis

Air film only analysis (structure assumed to be very stiff) with **Air Bearing Calculator**

- Takes away the effort of FEM modelling, analysis set-up and post-processing

AirBearing Calculator, v4



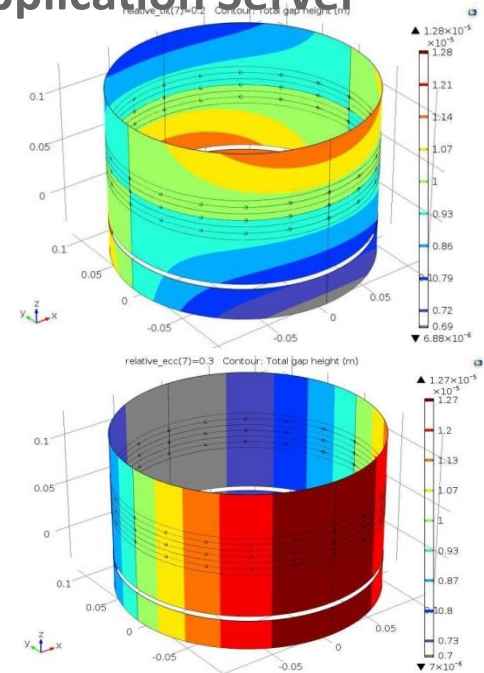
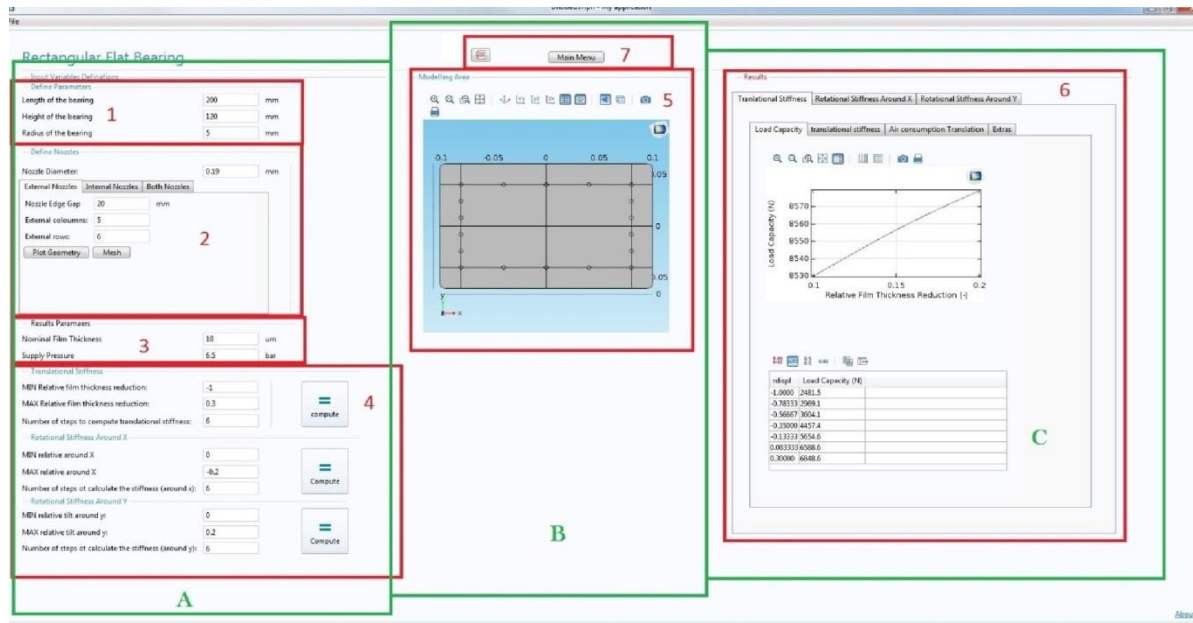
- ← Main page: Select configuration:
1. Rectangular/Cylindrical flat Air Bearing
 2. Cylindrical/Conical Air Bearing
 3. Under development: Flat Porous Air Bearing

Use of COMSOL within Development & Engineering

Example: Air Bearing Analysis

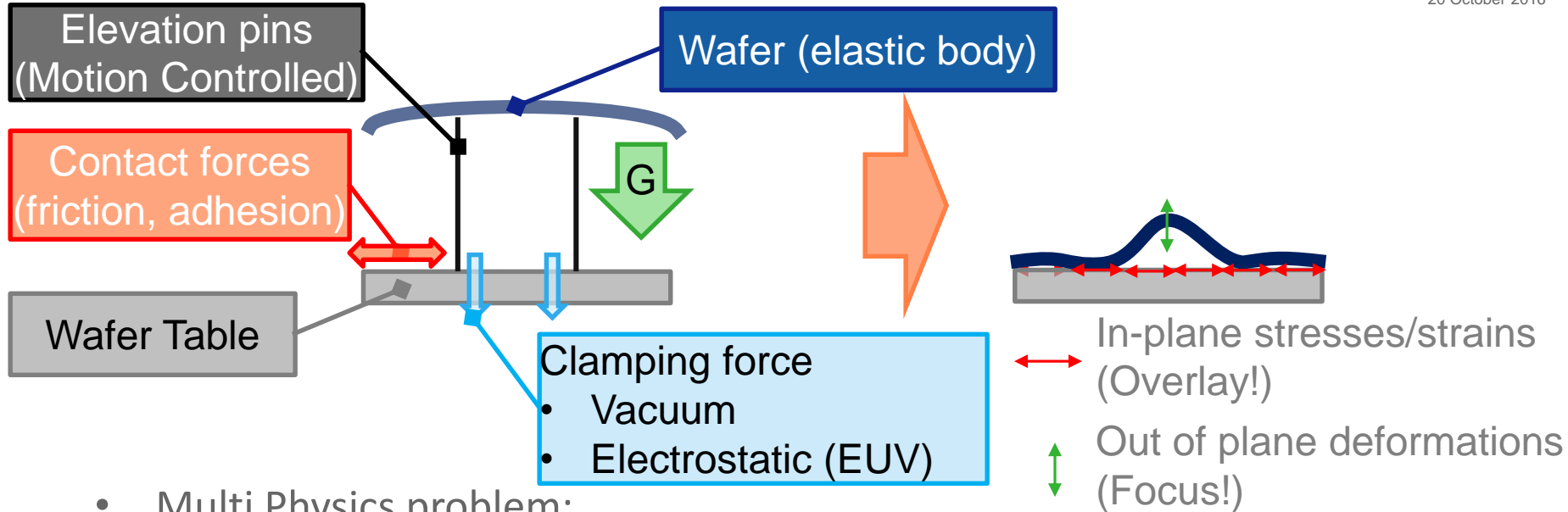
Air film only analysis (structure assumed to be very stiff)

- Input dimensions and other variables and results page
- Will be made available to more engineers via **COMSOL Application Server**



Use of COMSOL within Development & Engineering

Under development: Wafer Load Simulation



- Multi Physics problem:
 - (Wafer) Dynamics
 - Flow
 - Contact mechanics
 - Thermal
 - Electrostatics
 - Motion Control

Questions?



The image features the ASML logo in a bold, dark blue, sans-serif font. The logo is positioned on the left side of the frame. The background is a light blue gradient with abstract, flowing white lines that create a sense of movement and depth, resembling stylized waves or a modern architectural design.

ASML